# Bulusu Anand

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## Education

- Dec 2006: **Ph. D,** Electrical Engineering, Indian Institute of Technology, Bombay
- Jan 1998: **M. E** Electrical Engineering (Microelectronics), Birla Institute of Technology and Science, Pilani
- July 1995: **B. E,** Electronics and Communication Engineering, Andhra University, Visakhapatnam

## Current Research Interests:

- Novel device/circuit interaction
- Variation aware VLSI circuit design methodology
- Delay and timing models for VLSI circuits
- CMOS VCO Design and Modeling
- Near threshold VLSI circuit design

## Professional Background:

| From | To | Designation | Organisation |
|---|---|---|---|
| 2006 | 2007 | Sr. Research Engineer | IIT Bombay |
| 2007 | 2008 | Sr. Design Engineeer | Freescale Semiconductor India (Earstwhile Semiconductor Division of Motorola Inc., presently NXP Semiconductors) |
| 2008 | 2014 | Assistant Professor | IIT Roorkee |
| 2014 | 2019 | Associate Professor | IIT Roorkee |
| 2019 | Present | Professor | |

## Publications:

**Selected Publications in International Journals**:

1. Neeraj Mishra, Lalit M Dani, Kunal Sanvaniya, S. Dasgupta, S.Chakraborty, and Anand Bulusu, "Design and Realization of High-Speed Low-Noise Multi-loop Skew-based ROs Optimized for Even/Odd Multi-Phase Signals," Accepted for publication in IEEE TCAS-II.
2. Chaudhry Indra Kumar, and Bulusu Anand, "A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design", in IEEE Transactions on Device and Material reliability, 2019. (Early Access).
3. Chaudhry I. Kumar and Bulusu Anand, "A Highly Reliable and Energy Efficient Radiation Hardened 12T SRAM Cell Design, Accepted for pubilcation in IEEE Transactions on Device and Material Reliability.
4. Lalit Dani, N. Mishra, A. Sharma, Bulusu Anand, "Variation Aware Prediction of Circuit Performance in Near-threshold Regime using Supply Independent Transition Threshold Points," Accepted for publication in IEEE Transactions on Electron Devices.
5. C. I. Kumar and B. Anand, "A Highly Reliable and Energy Efficient Triple-Node-Upset Tolerant Latch Design", Accepted for publication in IEEE Transactions on Nuclear Science.
6. Abhishek Acharya, A. B. Solanki, S. Glass, Q. T. Zaho, and Bulusu Anand, "Impact of Gate-Source Overlap on the Device/ Circuit Analog Performance of Line TFETs," Accepted for publication in IEEE TED.
7. Shashank Banchhor, Kintada Dinesh Kumar, Ashish Dwivedi and Bulusu Anand, "A New Aspect of Saturation Phenomenon in FinFETs and Its Implication on Analog Circuits," Accepted for publication in IEEE TED.
8. Chaudhry Indra Kumar, Ishant Bhatia, Arvind Kumar Sharma, Deep Sehgal,H.S. Jatana, and Anand Bulusu, "A Physics based Variability Aware Methodology to Estimate Critical Charge for Near-Threshold Voltage Latches," Accepted for publication in IEEE Transactions on VLSI.
9. Chaudhry Indra Kumar and Bulusu Anand, "High Performance Energy Efficient Radiation Hardened Latch for Low Voltage Applications," Elsevier VLSI Journal of Integration, Accepted for publication.
10. Chaudhry Indra Kumar, Arvind Kumar Sharma, RajendraPartap, Anand Bulusu, "An energy-efficient variation aware self-correcting latch," Elsevier Microelectronics Journal, pp. 67 – 78, February 2019.
11. Chaudhry Indra Kumar and Bulusu Anand, "Design of highly reliable energy-efficient SEU tolerant 10T SRAM cell," IET Electronics Letters, pp. 1423 – 1424, December 2018.
12. Arvind Sharma, Naushad Alam and Anand Bulusu, "Effective Drive Current for Near-Threshold CMOS Circuits' Performance Evaluation: Modeling to Circuit Design Techniques," IEEE Transactions on Electron Devices, pp. 2413 – 2421, June 2018.
13. Abhishek Acharya, Abhishek Solanki, Sudeb Dasgupta and Bulusu Anand, "Drain Current Saturation in Line Tunneling-Based TFETs: An Analog Design Perspective," IEEE Transactions on Electron Devices, Volume: 65, Issue: 1, Jan. 2018..
14. Om Prakash , Satish Maheshwaram,Mohit Sharma Anand Bulusu , Sanjeev K. Manhas, "Performance and Variability Analysis of SiNW 6T-SRAM Cell using Compact Model with Parasitics," IEEE Transactions on Nanotechnology , Volume: 16, Issue: 6, Nov. 2017.

15. Arvind Sharma, Naushad Alam and Anand Bulusu, “Effective Current Model for Inverter-Transmission Gate Structure and Its Application in Circuit Design,” IEEE Transactions on Electron Devices, October 2017.
16. Om Prakash, Swen Beniwal, Satish Maheshwaram, Anand Bulusu, Navab Singh, and S. K. Manhas, “Compact NBTI reliability modeling in Si nanowire MOSFETs and effect in circuits,” IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, VOL. 17, NO. 2, JUNE 2017.
17. Abhishek Acharya, S. Dasgupta, Bulusu Anand, “A Novel VDSAT Extraction Method for Tunnel FETs and its Implication on Analog Design” IEEE Transactions on Electron Devices, February 2017.
18. Abhishek Acharya, S. Dasgupta, Bulusu Anand, “A novel VDSAT extraction method for tunnel FETs and its implication on analog design,” IEEE Transactions on Electron Devices, December 2016.
19. Arvind Sharma, Naushad Alam, Sudeb Dasgupta, Bulusu Anand, “Multifinger MOSFETs’ Optimization Considering Stress and INWE in Static CMOS Circuits”, IEEE Transactions on Electron Devices, PP, no. 99, 2016.
20. Baljit Kaur, Arvind Sharma, Naushad Alam, Sanjeev K. Manhas, Bulusu Anand, “A Variation Aware Timing Model for a 2-Input NAND Gate and Its Use in Sub-65nm CMOS Standard Cell Characterization”, Microelectronics Journal (Elsevier), vol. 53, pp. 45-55, 2016.
21. Archana Pandey; Harsh Kumar; S. K. Manhas; Sudeb Dasgupta; Bulusu Anand , “Atypical Voltage Transitions in FinFET Multistage Circuits: Origin and significance” , IEEE Transactions on Electron Devices, pp. 1392-1396, march 2016.
22. Baljit Kaur, Naushad Alam, S. K. Manhas, Bulusu Anand, “Efficient ECSM characterization considering voltage, temperature and mechanical stress variability,” IEEE Transactions on Circuits and Systems – I, pp. 3407-3415, December 2014.
23. Gaurav Kaushal, S. K. Manhas, S. Maheshwaram, S. Dasgupta, B. Anand, and N. Singh, “Novel Design Methodology Using Lext Sizing in Nanowire CMOS Logic” IEEE Transactions on Nanotechnology, pp. 650-658, July 2014.
24. Naushad Alam, Bulusu Anand and Sudeb Dasgupta, “An Analytical Delay Model for Mechanical Stress Induced Systematic Variability Analysis in Nanoscale Circuit Design,” IEEE Transactions on Circuits and Systems – I, pp. 1714-1726, June 2014.
25. Archana Pandey, Bulusu Anand, Swati Raycha, Satish Maheshwaram, S. K. Manhas, S. Dasgupta, “Effect of Load Capacitance and Input Transition Time on Underlap FinFET Capacitance,” IEEE Transactions on Electron Devices, pp. 30-36, January 2014.
26. Ashwani Kumar, Vishvendra Kumar, Bulusu Anand, S. Manhas, “Nitrogen-Terminated Semiconducting Zigzag GNR FET With Negative Differential Resistance,” IEEE Transactions on Nanotechnology, pp. 16-22, January 2014.
27. S. Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand and N. Singh, “Vertical Nanowire CMOS Parasitic Modeling and its Performance Analysis,” IEEE Transactions on Electron Devices, vol. 60, no. 9, pp. 2943-2950, Sept. 2013.
28. Menka, Bulusu Anand and Dasgupta S**.,** **“**Two Dimensional Analytical Modeling for Asymmetric 3T and 4T Double Gate Tunnel FET in Subthreshold Region: Potential and Electric Field**”,** Microelectronics Journal (In press).

29. N. Alam, B. Anand, and S. Dasgupta, “The Impact of Process-Induced Mechanical Stress in Narrow Width Devices and Variable Taper CMOS Buffer Design", Elsevier Microelectronics Reliability, vol. 53, Issue 5, pp. 718-724, May 2013.
30. N. Alam, B. Anand, and S. Dasgupta, “The Impact of Process-Induced Mechanical Stress on CMOS Buffer Design using Multi-Fingered Devices", Elsevier Microelectronics Reliability, vol. 53, Issue 3, pp. 379-385, March 2013.
31. N. Alam, B. Anand, and S. Dasgupta, "Gate-Pitch Optimization for Circuit Design using Strain-Engineered Multi-Finger Gate Structures", *IEEE Transactions on Electron Devices*, vol. 59, no. 11, pp. 3120-3123, November 2012.
32. Gaurav Kaushal, S. Manhas, S. Maheshwaram, S. Dasgupta, A. Bulusu and N. Singh, “Tuning source/drain extension profile in current matching in nanowire CMOS logic,” IEEE Transactions in Nanotechnology, vol. 11, no. 5, pp. 1033-1035, September 2012.
33. Satish Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand and N. Singh, "Device Circuit Co-Design Issues in Vertical Nanowire CMOS Platform," IEEE Electron Device Letters, vol.33, no. 7, pp.934-936, July 2012.
34. Satish Maheshwaram, S. K. Manhas, Gaurav Kaushal, Bulusu Anand, and Navab Singh, “Vertical Silicon Nanowire Gate-All-Around Field Effect Transistor Based Nanoscale CMOS,” IEEE Electron Device Letters, pp. 1011-1013, August 2011.
35. Pradeep Kumar Chawda, B. Anand, V. Ramgopal Rao, “Optimum Body Bias constraints for leakage reduction in high-K Complementary Metal Oxide Semiconductor Circuits,” Japanese Journal of Applied Physics (JJAP), May 2009.
36. Bulusu Anand, M. P. Desai, and V. Ramgopal Rao, "Silicon Film Thickness Optimization for SOI-DTMOS from Circuit Performance considerations", IEEE Electron Device Letters, pp. 436-438, June 2004.
37. P. Sivaram, B. Anand, M. P. Desai, “Silicon film thickness considerations for SOI-DTMOS,” IEEE Electron Device Letters, pp. 276-278, May 2002.

**IPs:**

1. Bulusu Anand, Shivananda Reddy, Surya Veeraraghavan, “A Method to Find Sensitivity of Standard Cells to Process/Model Changes,” Defensive Publication of Freescale Semiconductor Inc., June 2008, http://www.priorartdatabase.com/IPCOM/000172383/
2. S. K. Manhas, S. Nema, A. Bulusu, “A method of fabricating dual/asymmetric dielectric constant (dual-K) spacers in MOSFET,” application no. CINIITR000100017, 2012 (Provisional Indian Patent).

**Selected Publications in International Conferences:**

1. Lalit M. Dani, Neeraj Mishra and Anand Bulusu, “MOS Varactor RO architectures in Near Threshold Regime using Forward Body Biasing techniques,” VLSI Design Conference, January 2019, Delhi.
2. Lalit M. Dani, N. Mishra, S.K. Banchhor, S. Miryala, A. Doneria, Bulusu Anand, “Design and Characterization of Bulk Driven MOS Varactor Based VCO at Near Threshold Regime,” IEEE-S3S, San Francisco, October 2018.
3. Raghav Chawla, S. Yadav, A. Sharma, B. Kaur, R. Pratap and Bulusu Anand, “TSV Induced Stress Model and Its Application in Delay Estimation,” IEEE-S3S, San Francisco, October 2018.

4. Raghav Chawla, A. Sharma, N. Alam, Bulusu Anand, “Modeling the effect of variability on the timing response of CMOS inverter-transmission gate structure,” International Symposium on Devices, Circuits and Systems (ISDCS), Howrah.
5. C. Inder Kumar and Bulusu Anand “Design and Analysis of Energy-Efficient Self-Correcting Latches Considering Metastability,” IEEE PRIME, July 2018, Prague.
6. A. Sharma, N. Alam, A. Bulusu, “UTBB FD-SOI Circuit Design using Multifinger Transistors: A Circuit-Device Interaction Perspective,” IEEE PRIME, July 2018, Prague.
7. Archana Pandey, Pitul Garg, Shobhit Tyagi, Rajeev Ranjan, Anand Bulusu, “A Modified Method of Logical Effort for FinFET Circuits considering of Fin-Extension Efforts,” IEEE ISQED-2018.
8. Abhishek Acharya, Sudeb Dasgupta and Bulusu Anand, Impact of Device Design Parameters on $V_{DSAT}$ and Analog Performance of TFETs,” Accepted for presentation in IEEE Silicon Nanoelectronics Workshop 2017.
9. Archana Pandey, Harsh Kumar, Praanshu Goyal, S. K. Manhas, Sudeb Dasgupta, Bulusu Anand “FinFET Device Circuit Co-design Issues: Impact of Circuit Parameters on Delay” , IEEE VLSI Design, 2016.
10. Sayyaparaju Sagar Varma, A. Sharma, Bulusu Anand, "An efficient methodology to characterize the TSPC flip flop setup time for static timing analysis," IEEE SMACD, 2016, Lisbon.
11. Chaudhry Indra Kumar, A. Sharma, S. Miryala, Bulusu Anand, "A novel energy-efficient self-correcting methodology employing INWE," IEEE SMACD, 2016, Lisbon.
12. Arvind Sharma, Neeraj Mishra, Naushad Alam, Sudeb Dasgupta, and Bulusu Anand, "Pre-layout Estimation of Performance and Design of Basic Analog Circuits in Stress Enabled Technologies" in IEEE VDAT, 2015.
13. Yogesh Chaurasiya, Surabhi Bhargava, Arvind Sharma, Baljit Kaur, and Bulusu Anand, "Timing Model for Two Stage Buffer and Its Application in ECSM Characterization", in IEEE VDAT, 2015.
14. Arvind Kumar Sharma, Yogendra Sharma, Sudeb Dasgupta and Bulusu Anand, “Efficient Static D-Latch Standard Cell Characterization Using a Novel Setup Time Model,” Accepted in IEEE ISQED 2015.
15. Parmanand Singh,V. Asthana, R. Sithanandam, A. Bulusu, S. Dasgupta, “Analytical Modeling of Sub-onset Current of Tunnel Field Effect Transistor,” IEEE VLSI Design, 2014.
16. Bijay Kumar Dalai, A. Bulusu, N. Kannan and Arvind Kumar Sharma, "An Empirical Delta Delay Model for Highly Scaled CMOS Inverter Considering Well Proximity Effect," VDAT 2014.
17. Saurabh K. Nema, M. SaiKiran, P. Singh, Archana Pandey, S. K. Manhas, A. K. Saxena, Anand Bulusu, “Improved Underlap FinFET with Asymmetric Spacer Permittivities,” Accepted in IWPSD 2013.
18. Arvind Kumar Sharma, Naushad Alam, Sudeb Dasgupta and Bulusu Anand, “The Impact of Process-Induced Mechanical Stress on D-Latch Timing Performance,” Accepted in IEEE IMPACT 2013.
19. S. Maheshwaram, S.K. Manhas, G. Kaushal, and B. Anand, “Vertical Nanowire MOSFET Parasitic Resistance Modeling,” *in Proc. IEEE EDSSC* 2013, Hong Kong.
20. Prahlad Kumar Sahu, R. Sithanandam , Anand Bulusu and Sudeb Dasgupta “TCAD Evaluation of Fin Architecture on SOI Substrate and its Comparison with Planar FDSOI MOSFET at 28nm Technology Node”,” VDAT, 2013.

21. Menka, Bulusu Anand and Dasgupta S., "A TCAD approach to evaluate channel electrondensity of double gate symmetric n-tunnel FET", INDICON 2012, pp:577-581
22. Baljit Kaur, S. Miryala, S. K. Manhas and Bulusu Anand, "An Efficient Method for ECSM Characterization of CMOS Inverter in Nanometer Range Technologies," Accepted in IEEE International Symposium on Quality Electronic Design (ISQED) 2013.
23. Archana Pandey, Swati Raycha, Satish Maheshwaram, S. K. Manhas, S. Dasgupta, Bulusu Anand, "Underlap FinFET Capacitance: Impact of Input Transition Time and Output Load" IEEE International Nanoelectronics Conference (INEC) 2013.
24. N. Alam, B. Anand, and S. Dasgupta, "Process induced mechanical stress aware poly-pitch optimization for enhanced circuit performance", in *IEEE ISQED*, 2012, pp. 717-720.
25. N. Alam, B. Anand, and S. Dasgupta, "Impact of Dummy Poly on the Process-Induced Mechanical Stress Enhanced Circuit Performance", in *VDAT 2012*, pp. 357-359.
26. N. Alam, S. Dasgupta, and B. Anand "Impact of process-induced mechanical stress on multi-fingered device performance", in *Proc. IWPSD*, 2011.
27. Arnab Kumar Biswas, Anand Bulusu and Sudeb Dasgupta, "A Proposed Output Buffer at 90 nm Technology with Minimum Signal Switching Noise at 83.3MHz," Proceedings of IEEE ISVLSI 2011.
28. Sandeep Miryala, Baljeeth Kaur, Bulusu Anand and Sanjeev Manhas, "Efficient Nanoscale VLSI Standard Cell Library Characterization Using a Novel Delay Model," Proceedings of IEEE ISQED 2011.
29. Saurabh Nema, Mayank Srivastava, Angada B. Sachid, A. K. Saxena, Anand Bulusu, "A Novel Scaling Strategy for Underlap FinFETs," ICCCD 2010, IIT Kharagpur.
30. Bulusu Anand, V. Ramgopal Rao and M. P. Desai, "Circuit Performance Improvement Using PDSOI-DTMOS Devices with a Novel Optimal Sizing Scheme Considering Body Parasitics," Accepted in VLSI-DAT, 2007.
31. Pradeep Kumar Chawda, B. Anand, and V.Ramgopal Rao, "Effectiveness of Optimum Body Bias for Leakage Reduction in High K CMOS Circuits", Proceedings of 35th International Conference on Solid State Devices and Materials (SSDM 2004), pp. 434-435, Tokyo, Japan, September 15-17, 2004.
32. Sushant Suryagandh, B. Anand, M. P. Desai and V. Ramgopal Rao, "Dynamic Threshold Voltage CMOS (DTMOS) for Future Low Power Sub-1V Applications," Proceedings of 10th International Workshop on Physics of Semiconductor Devices (IWPSD), pp. 655-658, December 1999, New Delhi.

## Sponsored Projects:

1. "Nanoscale FinFET device and circuit design methodology"
PI: Anand Bulusu Sponsor: DST Cost: Rs. 20.40 Lakh Status: Completed
Description: We developed **a quantitative link between device and circuit level performance of FinFETs**. We developed models of FinFET device parasitics and using these to develop circuit delay models.

2. "A robust methodology for nanoscale VLSI circuit design considering layout dependent systematic variations"
PI: Anand Bulusu, Co-PI: Sudeb Dasgupta Sponsor: DST Cost: Rs. 38.37 Lakh Status: Final report submitted to DST

Description: Our aim in this project is to **model timing performance parameters of circuits with layout parameters** in CMOS technologies having process induced mechanical stress. Using such models, we would propose methods to improve the performance of circuits in such CMOS technologies.

3. "Remote Detection of Humans Trapped Under Debris in Disaster Affected Areas Using RF Sensing of Cardiopulmonary Motion." (SMPD-C2SD)
PI: Sudeb Dasgupta, Co-PI: Anand Bulusu Sponsor: MIETY (formerly DIETY) Cost: Rs. 5 Cr. Status: Ongoing
Description: In this project, we propose an RF sensing based system which can identify the number and depths of living persons trapped inside debris due to disasters such as earthquakes etc. The presence of human life can be ascertained by the virtue of its vital signs such as respiration rate and heartbeats. We propose to use a system applying single band RF sensors with on-chip processing. All the parts of the system (except PA and antenna) would be implemented within a CMOS SoC. My contribution is more in the **CMOS circuit development aspects** of the project.

4. ICT Academy
PI: Sanjeev Manhas Co-PI: Anand Bulusu Sponsor: MIETY (formerly DIETY) Cost: Rs. 7 Cr. Status: Ongoing
Description: In this project, the faculty and graduates of academic institutions in Uttarakhand, Himachal and Jammu and Kashmir would be imparted course and skill training.

5. Advanced MOS Physics and its application to device modeling (Consultancy)
PI: Anand Bulusu Sponsor: SCL, Chandigarh, ISRO Cost: Rs. 1.7 Lakh Status: Completed
Description: Classes and discussion on advanced MOS physics and modeling for SCL's CMOS technology.

6. Development and Efficient Characterization of Floating Body (FB) and Dynamic Threshold (DT) CMOS Partially Depleted Silicon-On-Insulator (PDSOI) Standard Cell Libraries
PI: Anand Bulusu Sponsor: DST Cost: Rs. 59 Lakhs Status: Ongoing
Description: PDSOI technology is being developed in India by SCL Chandigarh for its radiation hard nature. The project aims for the **design enablement of the PDSOI technology and its early circuit design for process and PDK improvement**. We will consider the PDSOI floating body effects rigorously.

7. An energy efficient IoT processor build using an optimized near-threshold voltage standard cell library
PI: Anand Bulusu Sponsor: IMPRINT-2 (DST) Cost: Rs. 54 Lakhs Status: Ongoing
Description: This project involves the development of **a near threshold standard cell library** an IoT processor in a 28 nm CMOS process and in SCL's 180 nm CMOS process.

8. A Robust and Scalable VLSI Standard Cell Characterization Methodology for High Performance CMOS Designs Considering Spatial and Temporal Variations
PI: Anand Bulusu Sponsor: Semiconductor Research Corporation (SRC) Cost: $34321 Status: Ongoing

Description: **Timing models of planar, FinFET standard cells would be developed**, considering interconnects. These would estimate spatial and temporal variations through Vth, μ0 and RCs.

9. A PDSOI Analog cell library consisting 2-stage OPAMPs and comparators designed considering Floating Body (FB) and self-heating (SH) effects
PI: Anand Bulusu Sponsor: ISRO Cost: Rs. 19 Lakhs Status: Recommended by ISRO RESPOND for funding by ISRO-IITR STC
Description**: Floating-Body and Self-Heating effects would cause the operating point of PDSOI analog circuits to be an asymptotically settling transient**. This project would deliver a basic analog cell library considering these effects in the design methodology.

10. "Negative capacitance FET (NCFET): fabrication, modeling and simulation for a systematic design of digital circuits"
PI: Arnab Dutta Co-PI: Bulusu Anand Co-PI: Sudeb Dasgupta Co-PI: Sanjeev Manhas
Sponsor: DST (Nano Mission) Cost: Rs. 1.13 Crore Status: Ongoing
Description: Negative capacitance (NC) FET devices are one of the main candidates for future VLSI technologies. However, **a circuit design methodology needs to be devised** considering the impact of their ferro-electric layer's polarization with respect to the device's drain bias and transient voltages. My contribution would be in this aspect of the project.

## Visits:

Visited Forschungszentrum, Julich, Germany in June – July (2 months) 2018 under **DAAD Bilateral Faculty Exchange Program** to collaborate on Negative Capacitance FETs and TFETs. My German collaborator, Prof. Q-T. Zhao, visited IIT Roorkee in December 2018.

## Ph.Ds Supervised:

| Area | Name | Status | Funding | Joint/Single supervision | Current Employment |
|---|---|---|---|---|---|
| Variation Aware Efficient Standard Cell Characterization | Lomash Acharya | Ongoing | Project Staff | Joint (main supervisor) | - |
| Near Threshold Standard Cell Design | Mahipal D. | Ongoing | Project Staff | Joint (main supervisor) | - |
| NCFET Device Circuit Interaction | Amit Bahera | Ongoing | Project Staff | Joint (main supervisor) | - |
| NC-Tunnel FET Device Circuit Interaction | Khoiram Johnson | Ongoing | DST-INSPIRE | Joint (co-supervisor) | - |
| Radiation Hard Circuit Design at Cryogenic Temperature | Ashutosh Yadav | Ongoing | ISRO Sponsored | Joint (main supervisor) | ISRO |

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|---|---|---|---|---|---|
| Analog Circuit Design in PDSOI technologies | H. S. Jatana | Ongoing | ISRO Executive | Joint (main supervisor) | ISRO |
| Circuit Design for In-Memory Computation | Dinesh Kushwaha | Ongoing | MHRD | Joint (main supervisor) | - |
| NCFET Device-Circuit Interaction | Nitanshu Chauhan | Ongoing | NIT Uttarakhand | Joint (main supervisor) | NIT Uttarakhand |
| FinFET Device-Circuit interaction (Analog Domain) | Shashank Bancchor | Ongoing | MHRD | Single supervision | - |
| FinFET Device-Circuit interaction in Near Threshold Digital Domain | Sarita Yadav | Ongoing | NIT Uttarakhand | Single supervision | NIT Uttarakhand |
| CMOS PLL Design | Neeraj Mishra | Ongoing | SMDP-C2SD | Single supervision | - |
| Low Voltage CMOS VCO Design | Lalit Dani | Ongoing | CSIR-NET SRF | Single supervision | - |
| Near Threshold CMOS Digital Circuit Design and Analysis | Inder Chaudhary | Awarded | MHRD | Single supervision | Project |
| Tunnel FET Device-Circuit Interaction | Abhishek Acharya | Awarded | QIP | Single supervision | NIT Surat |
| Mechanical Stress Aware Nanoscale VLSI Circuit Design Methodologies | Arvind Sharma | Awarded | Project Staff | Single supervision | Post-Doc, Univ. Minnesota |
| Modeling of FinFET device parasitics | Archana Pandey | Awarded | MHRD | Single supervision | J. P. University |
| TunnelFET device-circuit co-design | Menaka | Awarded | QIP | Joint (co-supervisor) | NIT Jaipur |
| Device-circuit co-design of Silicon Nanowire transistor | Satish Maheshwaram | Awarded | MHRD | Joint (co-supervisor) | NIT Warangal |
| Performance models for nanoscale VLSI circuits | Baljit Kaur | Awarded | MHRD | Joint (main supervisor) | NIT Delhi |
| Robust circuit design methodology for nanoscale VLSI technologies | Naushad Alam | Awarded | Sponsored | Joint (main supervisor) | AMU |

## **Ph.D Thesis**:

**Evaluating DTMOS in solving the voltage scaling problem: A circuit performance perspective**

**Supervisor:** Prof. Madhav P. Desai, EE Department, IIT Bombay.

Increasing circuit speed by scaling is resulting in the problem of exponentially increasing the leakage power in sub-1V technologies. One of the proposed solutions to this problem is Dynamic-Threshold-MOSFET (DTMOS), which is also compatible with conventional CMOS technology. In DTMOS, a forward bias is applied to the body of a MOSFET when it is ON. This results in an increased drive current in a DTMOS device while the leakage current is not affected. However, a study of its impact at the circuit level, while considering the DTMOS device bodies in detail, has not been done thus far. In this work we compare the performance of an optimized DTMOS circuit with that of its conventional equivalent while considering the loading and parasitic effects of the DTMOS device body. We first optimize the DTMOS device design such that circuit performance is maximized. For this, we propose a novel figure-of-merit (FoM) for the device and show that by optimizing this FoM we obtain device design parameters which maximize logic gate performance. We must now compare the projected performance of DTMOS and conventional implementations of an arbitrary logic circuit. For this, we derive simple but accurate delay and input capacitance models for DTMOS logic gates. These delay models incorporate the effect of the body parasitics, and can be used to project the behaviour of logic circuits. Thus, in our work, we establish a quantitative link between DTMOS device performance and circuit level performance. Based on this approach, in a 50nm drawn gate length technology, we conclude that DTMOS is a *partial* solution to the voltage scaling problem and can be used to reduce the leakage power significantly if an overhead in area can be tolerated. We also observe that in PDSOI technology, the DTMOS device can be more effective than the body-tied-to-source device in eliminating the floating body (FB) and kink effects, if the area overhead can be tolerated.

## Pre-IITR Research Experience:

- Jul 2006 – March 2007 (Indian Institute of Technology, Bombay)

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|---|---|
| **Project Name** | Comparison of performance of CMOS and NMOS technologies |
| **Designation** | Senior Research Engineer |
| **Supervisor** | Prof. V. Ramgopal Rao |
| **Description** | The aim of this project is to explore if NMOS logic can reduce power consumption as compared to CMOS. This involves optimizing threshold voltages of devices for NMOS logic, optimizing NMOS circuits and comparing representative NMOS and CMOS circuits. |

March 2007 – April 2008 (Freescale Semiconductor India Pvt. Ltd.)

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|---|---|
| **Project Name** | A metric for sensitivity of standard cells to process variations |
| **Designation** | Senior Design Engineer |
| **Supervisor** | Dr. Surya Veeraraghavan and Dr. Bhuwan Agarwal |

**Description** Process parameters keep changing due to a gradual "maturing" of technology. The aim of this project is to propose a "metric" for each standard cell, which can give a "measure" of sensitivity of its delay/power characteristics to process variations at each corner.

- November 2007 – February 2008 (Freescale Semiconductor India Pvt. Ltd.)

**Project Name** Optimum standard cell design in sub-100nm CMOS LP technologies
**Designation** Senior Design Engineer
**Supervisor** Dr. Surya Veeraraghavan and Dr. Bhuwan Agrawal
**Description** In Low Power (LP) CMOS, technologies, the value of local interconnect capacitance is also larger relative to other contributors. Due to these effects, traditional design and layout methodologies for standard cell library fail to produce desired performance. We proposed a method of standard cell design and layout for sub-100nm LP CMOS technologies.

- March 2008 – November 2008 (Freescale Semiconductor India Pvt. Ltd)

**Project Name** Impact of WPE and sress effects in 45nm CMOS circuits
**Designation** Senior Design Engineer
**Supervisor** Dr. Surya Veeraraghavan and Dr. Bhuwan Agrawal
**Description** Starting from 65nm bulk and PDSOI CMOS technologies, MOSFET instance parameter related to Well-Proximity Effect (WPE), stress effect and polysilicon corner rounding are being extracted from layout. However, this increases the time of extraction significantly. In this project, we would study the circuit impact of these effects from measured Silicon data obtained from several ring-oscillators in a test-chip. Our goal is to propose cases, if any, in which the extraction of these parameters is not needed.

## Collaboration/Joint Work with Industry:

| Topic | Organisation |
|---|---|
| Process variation aware Standard Cell extraction | Freescale Semiconductor India Pvt. Ltd. |
| Tunnel FET Device Modeling | ST Microelectronics |
| CMOS VCO Design | ST Microelectronics |
| High Speed Circuits | Global Foundries |
| SRAM Memory Reliability | ARM |
| AI Chip Design | Proficient Design LLC, USA |

| | |
|---|---|
| Near Threshold Voltage Library Design | Einfochips, SCL Chandigarh |

## Teaching Experience:

- Digital VLSI Circuit Design (PG + UG)
- Analog VLSI Circuit Design (PG + PG)
- Analog Circuits (UG)
- Semiconductor Devices (UG)
- Fundamentals of Microelectronics (UG)
- Fundamentals of Electronics (UG)
- Network Theory (UG)
- Automatic Control Systems (UG)
- Microelectroncs Devices, Circuits and Technology (UG Lab)
- IC Applications Lab (UG)

## Other Relevant Experience

- Our group has designed and is presently doing measurements on a *testchip* built in ST Microelectronics 65 nm CMOS node. The testchip has test structures to evaluate our designs and methodologies systematic variation aware circuit design, near threshold latches/FFs and VCOs.
- Designed a 0.25µm bulk technology *testchip* with DTMOS circuits. The chip also contained test circuits to validate a technique for interconnect coupling capacitance measurement (CBCCM). The test-chip was fabricated by TSMC and was characterized in IIT Bombay.
- Worked with SPICE, process simulators (TSUPREM4, ISE-DIOS, 3-D TAURUS PROCESS), device simulators (MEDICI, ISE-DESSIS), Layout Editors (MAGIC and Cadence Virtuoso), Schematic Editors, Layout-vs.-Schematic tools.
- Reviewer of research publications for in IEEE Transactions on Electron Devices, IEEE Electron Device Letters, ISLPED, A-SSCC, VLSI Design Conference etc
- Faculty advisor of IEEE Student Branch, IIT Roorkee and IEEE CAS Student Chapter, IIT Roorkee, Treasurer, IEEE SSC/CAS Joint Chapter, UP Section.
- Convener of Microelectronics and VLSI group, ECE Department, IIT Roorkee.

## Pre-Ph.D Work Experience

- October 1995 - June 1996 (Geonics India Pvt. Ltd., Mumbai)
  **Designation**: Engineer
  **Description**: My job was to maintain and assist in designing marine instrumentation systems for laying underwater pipelines in the Gulf of Kutch.

- February 1998 – October 1998 (IBM Global Services India Pvt. Ltd., Bangalore)
  **Designation**: Design Engineer
  **Description**: I was responsible for modifying the layout of 0.35µm standard cell library cells after the technology was improved to use Copper interconnect instead of the earlier Aluminum interconnect lines.

## References

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